Ionizing Radiation and Hot Carrier Effects in SiC MOS Devices

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We performed comparative studies of radiation-induced interface trap generation at n-6H-SiC/SiO_2 and Si/SiO_2 interfaces for high doses of low energy x-rays in the range 0 to 200 Mrad (Si). We found that radiation-induced interface trap generation at the n-6H-SiC/SiO_2 interface is much lower than at the Si/SiO_2 interface. The experiments provide evidence of interface trap generation near the SiC conduction band associated with oxide traps.

A microscopic model of radiation-induced defects in SiC MOS devices is still missing and further investigation is necessary [1]. In this work, we performed comparative investigations of ionizing radiation and hot carrier effects in SiC and Si MOS devices. We will report on experiments involving interface and oxide trap generation in the oxide and briefly discuss the mechanisms responsible for these effects.

Si MOS capacitors were fabricated using n-type 2 in., (100) silicon wafers of resistivity 1 Ω-cm. The wafers were cleaned by a modified RCA process as described elsewhere, yielding devices with radiation hardness improved by up to one order of magnitude [2]. Thermal oxides were grown in dry O_2 at 1000°C, followed by an in situ dry N_2 annealing for 30 minutes. Aluminum films approximately 200 nm thick were thermally evaporated to form gate electrodes. After backside metallization, the wafers were annealed in forming gas at 400°C for 30 minutes. This is an optimized fabrication process yielding devices with improved radiation hardness. On the other hand, the processing of the SiC MOS devices was not optimized and the devices are not expected to have the best radiation hardness possible. SiC MOS capacitors were fabricated on a 3.5° off-angled n-type 6H-SiC wafer (Si face) with a 5-microns-thick epitaxial layer. The nominal doping density of the epilayer is 6×10^{15} cm^{-3}. The wafers were ultrasonically cleaned in successive, five-min steps in methanol, acetone and 10% HF with a two-min rinse in deionized water between steps. The oxidation was performed in dry O_2 at 1000°C for 13 hours, followed by an in situ dry N_2 annealing for 30 minutes at the growth temperature. Aluminum was evaporated to form gate electrodes with a diameter of 1 mm and a large area back contact. The post-metallization annealing was done at 400°C in a mixture of 75% Ar-25% H_2 during 30 minutes. Irradiation source was a x-ray beam generated from a Cu target bombarded by 40 keV electrons (20 mA) and the dose rate was 6 Mrad(Si)/h. Most of the absorbed dose results from the radiation near 10 keV. The x-ray dose was previously evaluated by means of dosimeters, which consist in Si photodiodes with an aluminum gate of specified thickness (200 nm). Irradiated samples always have aluminum gates with same electrode thickness (200 nm), so that the effective x-ray dose in the oxide is known. The capacitors were in open-circuit condition during irradiation. Carrier injection was performed by means of a HP 4155A Semiconductor Parameter Analyzer.

Exposure to ionizing radiation or hot carrier injection cause increasing degradation of Si- and SiC- based devices due to the generation of interface trap and oxide defects, as depicted in figures 1 and 2. Fig. 1 shows that after Fowler-Nordheim injection of electrons into the oxide, the current density increases in the direct and Fowler-Nordheim tunneling regimes. This increment in current is mostly associated with the generation of oxide traps, which assist the tunneling process. Oxide trap generation leads to oxide charging, soft and hard breakdown of the oxide. Oxide thickness and gate area

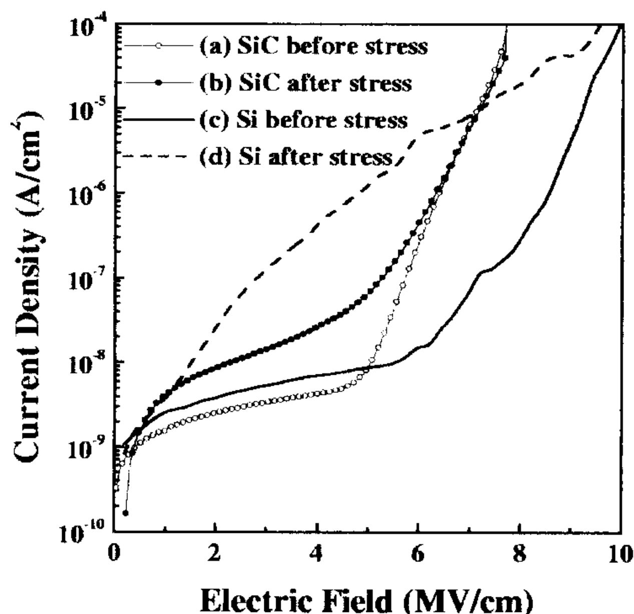

Figure 1. Current characteristics of SiC and Si MOS capacitors after repeated positive voltage ramp stressing (seven cycles, current limit set to 1μA).

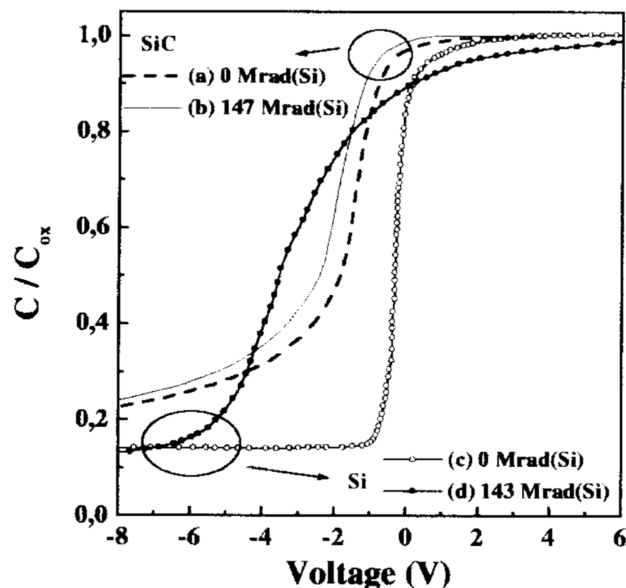

Figure 2. Capacitance-voltage characteristics of a Si MOS and a SiC MOS capacitor irradiated with similar x-ray doses.

are respectively: 50 nm and 3.02×10^{-3} cm^2 (curves (a) and (b)) and 10 nm and 3.6 $\times10^{-3}$ cm^2 (curves (c) and (d)). Fig. 2 shows room temperature capacitance-voltage characteristics of Si and SiC MOS capacitors irradiated with similar x-ray doses. Oxide thickness of the n-6H-SiC MOS capacitor (curves (a) and (b)) is 85 nm, gate area is 7.85×10^{-3} cm^2. Oxide thickness of the Si MOS capacitor (curves (c) and (d)) is 50 nm, gate area is 1.22×10^{-2} cm^2. In Fig. 1, one can see a reduced leakage current generation in the SiC MOS device and analyzing the high-frequency capacitance-voltage (CV) curves in Fig. 2, it is clear that the negative voltage shift, reflecting the generation of positive oxide charge and the stretch-out of the curves, reflecting the generation of interface states, are much reduced in the SiC MOS capacitor. This striking difference in behavior after exposure to ionizing radiation was the main focus of this investigation. In order to estimate the total interface trap density, we used both the stretch-out technique and the photo-capacitance-voltage method (also known as the Jenq technique) [3], by illuminating the capacitors with intense white light from fiber optic illuminators for 5 to 10 minutes. We used room-temperature quasistatic CV curves to check the quality of the oxide and to get a qualitative picture of the interface-trap generation. At room temperature, due to the large band gap of SiC, minority carrier generation is very low and SiC behaves in similar way as Si at lower temperatures, so that the energy range probed by the high-low technique is reduced to energies very close to SiC conduction band, or equivalently, very close to accumulation. This region of the spectrum has been ascribed to oxide traps [1].

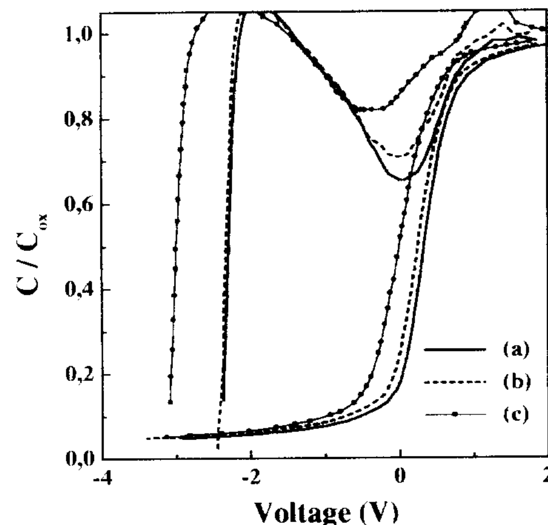

Figure 3. Capacitance-voltage curves of a 6H-SiC MOS capacitor exposed to different x-ray doses. Oxide thickness is 9 nm and gate area is 7.85×10^{-3} cm^2. Doses in Mrad(Si) are: (a) 0, (b) 14, (c) 110.

Fig. 3 shows high frequency and quasistatic CV curves of a SiC MOS capacitor exposed to different x-rays doses. As in Fig. 2, the negative voltage shift of the high-frequency CV curves, reflecting the generation of positive oxide charge is low. Most of the variation in the quasistatic curves appears near the accumulation region. This variation is probably due to the generation of interface states in the upper range of the SiC band gap, since the energy range probed by the technique is reduced to energies very close to SiC conduction band. Therefore, the variation observed in the quasistatic curves implies defect generation near the conduction band. States deeper into the bandgap are not detected and nothing can be said about them.

Current peaks and misalignment are also observed. Current peaks near flatband are observed in devices with oxides heavily contaminated with mobile ions [5]. At elevated temperatures, when the oxide field reverses sign, the ions move and a peak in the displacement current appears. At room temperature, movement of the ions is reduced and we are led to believe that the current peaks are possibly related to oxide-trapped charges generated by irradiation and exchanging charge with the substrate, the so-called border traps or, equivalently, switching oxide traps [6]. Further investigation is needed to separate unambiguously the effect of the oxide traps from the effect of the mobile ions.

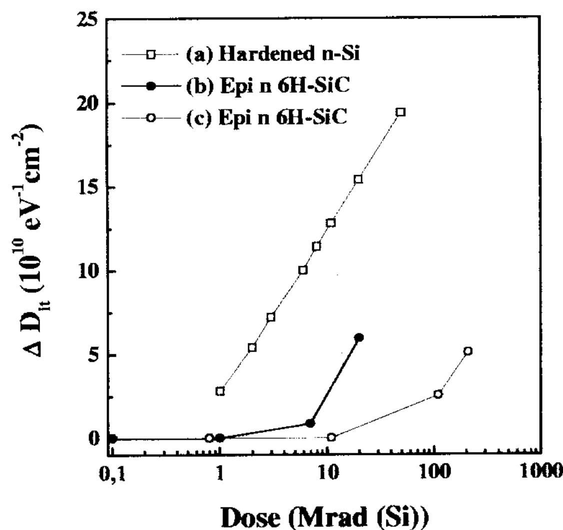

Figure 4. Interface trap generation in n-type 6H-SiC and Si MOS capacitors. Curve(a) is a previously reported result obtained in n-type Si under similar irradiation conditions, as discussed in the text. Oxide thickness is 23 nm (curve (a)), 85 nm (curve (b)) and 9 nm (curve (c)).

Fig. 4 shows interface trap generation (ΔD_{it}) as a function of dose compared with a previously reported result obtained in n-type Si under similar irradiation conditions (curve(a)). Curve (a) is the response of a commercial radiation-hard device (23 nm gate oxide) exposed to 10 keV x-rays at a dose rate of 18 Mrad (Si)/h with gate voltage equal to zero [4]. It is known, for Si devices, that the number of radiation-induced interface traps increases as the oxide thickness increases. Such a dependence on oxide thickness is also observed for the SiC devices, as shown in Fig. 4. However, it is clear that the SiC MOS capacitor has lower interface trap buildup, despite its oxide being almost four times thicker (85 nm) than the oxide of the commercial hardened (23 nm) Si device. The SiC MOS is radiation-hard even without adopting radiation-hardening procedures. These results are consistent with previous reports, performed using lower doses of radiation, showing promising radiation hardness for SiC devices [7]. Radiation-induced holes and hydrogen ions migrating towards the Si/SiO_2 interface play a very important role in the formation of interface traps. It is known that a relatively thick (20 nm) negative charge layer has been observed in 6H-SIC MOS capacitors [7]. So, one possibility to explain improved radiation hardness in SiC MOS devices is to admit that a mechanism of annihilation or charge compensation occurs near or at the SiC/SiO_2 interface, therefore preventing the formation of interface traps by holes and hydrogen ions. The oxide traps generated by these compensation/annihilation reactions near the interface could act as oxide-trapped charges that exchange charge with the substrate, possibly causing peaks in the quasistatic CV curves.

In summary,comparative x-ray irradiation of epitaxial 6H-SiC MOS capacitors and Si MOS capacitors showed that interface trap generation rate is much reduced in SiC MOS devices. Evidence of interface trap generation near the SiC conduction band associated with switching oxide traps could be observed. The radiation response of SiC devices, under x-ray exposure, indicated a much higher radiation immunity than in Si devices, despite the fact that the SiC devices were not specially processed to be radiation hard.

Acknowledgments

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