Foreword - The SiO_2-Si Interface

With the push for faster and more dense metal-oxide-semiconductor field-effect transistors (MOSFET), processor devices have progressed to the point where the needs of microelectronics technology, specially concerning the materials to be used as gate dielectric, are now beyond our understanding of either the fabrication of ultra-thin dielectrics or their basic electronic properties. For technologies beyond the 0.1 μm CMOS regime, gate dielectrics will be of the order of 3 nm or less. A thickness variation of 0.1-0.2 nm in these films can cause a shift in the leakage current over many orders of magnitude. The gate stack, and specifically the gate dielectric is a critical process module for the present and future of microelectronics technology, and may well be the determining factor that limits the further reduction on the dimensions of MOSFETs. One estimates presently that around eighty percent of the problems originated by the instabilities in MOSFET silicon devices are caused by the degradation of the gate dielectrics, when its thickness is scaled below 9 nm.

This industrial scenario gave origin in the last few years, to a very intense, worldwide research activity in the physics and chemistry of ultrathin films of SiO_2 on Si and of the SiO_2-Si interface. New and powerful experimental and numerical simulation methods have been used to investigate key issues like the mechanisms of thermal growth of ultrathin films of SiO_2 on Si, the defects structure at the interface, and the dielectric behavior of the SiO_2 films. More recently the defects structure of the SiO_2 film surface has also been investigated, as it affects the performance of the gate dielectric. The question to which an answer is being searched is: what is the ultimate limit to which these films can be scaled? In order to find out this answer, it is necessary to clarify: "what will be the controlling factor for the thickness limitation"? Will the thickness be limited by the transistor leakage current, process integration issues, or even the dielectric lifetime?

This challenging area of research in the nanometric and subnanometric world is described in this Section by outstanding authors, giving a broad view of the main facts, models, and future prospects for research. The articles are updated approaches to the corresponding specialties, and should have a stimulating effect on the scientific activity in the field.

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